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10/27/00 JC921 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
P4928/06145.003001

Total Pages in this Submission

JC813 U.S. PTO
09/698622
10/27/00

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC

and invented by:

Jyh-Ming JONG and Leo YUAN

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **11** pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☐ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

22511
PATENT TRADEMARK OFFICE

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
P4928/06145.003001

Total Pages in this Submission

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☐ Formal Number of Sheets _____
   b. ☒ Informal Number of Sheets 2
4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☐ With Power of Attorney ☒ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

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Docket No. P4928/06145.003001
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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☒ Additional Enclosures *(please identify below):*

Power of Attorney (1 page)

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

17. ☐ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

Warning

An applicant who makes a request not to publish, but who subsequently files in a foreign country or under a multilateral international agreement specified in 35 U.S.C. 122(b)(2)(B)(i), must notify the Director of such filing not later than 45 days after the date of the filing of such foreign or international application. A failure of the applicant to provide such notice within the prescribed period shall result in the application being regarded as abandoned, unless it is shown to the satisfaction of the Director that the delay in submitting the notice was unintentional.

UTILITY PATENT APPLICATION TRANSMITTAL
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Docket No. P4928/06145.003001
Total Pages in this Submission

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	13	- 20 =	0	x	$18.00	$0.00
Indep. Claims	5	- 3 =	2	x	$80.00	$160.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$710.00
OTHER FEE *(specify purpose)*	Assignment Fee					$40.00
					TOTAL FILING FEE	$910.00

☒ A check in the amount of **$870.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **500-591** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: 12/27/06

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CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Jyh-Ming JONG et al.**			Docket No. **P4928/06145.003001**
Serial No.	Filing Date	Examiner	Group Art Unit

Invention: **NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC**

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Beri Hartwell
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CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Jyh-Ming JONG et al.**	Docket No. **P4928/06145.003001**

Serial No.	Filing Date	Examiner	Group Art Unit

Invention: **NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC**

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PATENT
ATTORNEY DOCKET NO.: P4928/06145.003001

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: **NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC**

APPLICANTS: **Jyh-Ming JONG and Leo YUAN**

NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC

BACKGROUND

In digital signaling, the voltage swing of the signal often encounters significant noise. This is especially the case with low voltage signals at a high speed interface. In such applications, problems such as power noise or ground noise can be the result of simultaneous switching of input/output (I/O) buffers, signal reflections, or signal cross-talk. Noise can also result from a weakened physical interconnection caused by a bad solder joint, an improper connection, etc. The result of such noise is the reduction of signal voltage margin as well as degradation of signal performance and reliability.

Figure 1A shows a graphical depiction of an example of an ideal signal 10. The graph represents the voltage of the signal as depicted over time. VREF represents the mid-point reference of the voltage. VREF_L represents the lower voltage boundary. Any signal voltage level below this point, is considered a LOW signal value. VREF_H represents the high voltage boundary. Any signal voltage level above this point is considered a HIGH signal value.

In Figure 1A, the signal 10 starts LOW and transitions to HIGH before returning to LOW. The signal 10 clearly and unambiguously makes the successful transition in signal value. However, Figure 1B shows the effect on the signal 20 of noise caused by a ground glitch. The signal 20 never clearly makes the transition from LOW to HIGH. Instead, it is stuck in the transitional area between VREF_L and VREF_H. Figure 1C shows the effect on the signal 30 of noise caused by a power glitch. The signal 30 never clearly makes the transition from HIGH to LOW. As with the ground glitch of Figure 1B, the signal is stuck in the same transitional area without a clear, discernable value. Finally, Figure 1D

shows an example of the effect of a high resistance path. The signal 40 never crosses VREF_L during its transition from HIGH to LOW. As seen in the previous examples, its value it indeterminate.

In general, electrical characterization of noise related problems require proper software support in generating data patterns and robust hardware support to determine the transient voltage. A common method of debugging a system involves pin by pin testing to find signal voltage errors. This is a very costly and time-consuming operation whether in the laboratory, in the production facility, or in the field.

SUMMARY OF INVENTION

In some aspects the invention relates to an apparatus for detecting a noise error of a signal comprising: a high comparator that references a high voltage limit with the signal and generates an output; a low comparator that references a low voltage limit with the signal and generates an output; and a circuit that processes the high comparator output and the low comparator output, wherein the circuit generates an alarm if a noise error is detected.

In an alternative embodiment, the invention relates to an apparatus for detecting a noise error of a signal comprising: means for detecting a high voltage noise error; means for detecting a low voltage noise error; and means for activating an alarm signal upon detection of the high voltage or the low voltage noise error.

In an alternative embodiment, the invention relates to a method for detecting a noise error of a signal comprising: comparing a high signal voltage with a high reference voltage; activating an alarm if the high signal voltage is less

than the high reference voltage; comparing a low signal voltage with a low reference voltage; and activating an alarm if the low signal voltage is greater than the low reference voltage.

The advantages of the invention include, at least, the ability of a digital circuit to perform a self-diagnosis of signal noise error without pin-by-pin or other time intensive debugging methods. Another advantage of the disclosed invention includes the ability for the circuit to perform self-diagnosis of signal noise error in the test lab, at production quality control, or during actual usage.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1A shows a graph of an ideal signal voltage.

Figure 1B shows a graph of a signal voltage affected by ground glitch noise.

Figure 1C shows a graph of a signal voltage affected by power glitch noise.

Figure 1D shows a graph of a signal voltage affected by high resistance of the signal path.

Figure 2 shows a schematic of one embodiment of a noise margin self-diagnostic receiver circuit.

DETAILED DESCRIPTION OF THE INVENTION

Exemplary embodiments of the invention will be described with reference to the accompanying drawings. Like items in the drawings are shown with the same reference numbers.

Figure 2 shows a schematic of one embodiment of noise margin self-diagnostic receiver circuit. The receiver includes a data signal comparator 52 and a noise margin self-diagnostic circuit 50. The data comparator 52 receives a data

input 54 and generates an output 56 with respect to a predetermined reference voltage (VREF) for the signal. The self-diagnostic circuit 50 includes: two additional comparators 58, 60; two delay buffers 68a, 68b; four "flip-flop" circuits 62a - 62d; two "exclusive or"(XOR) logic gates 64a, 64b; a "not or" (NOR) logic gate; and a flag output 70.

In this embodiment, the data comparator 52 is a normal single ended data receiver. The comparator 52 itself may be a differential amplifier or a sense amplifier. The output of the comparator 52 is determined by whether the voltage of the data input signal 54 is higher or lower than the VREF. The comparison is made within an offset range. In some embodiments, the offset range may be ± 30mV. The other comparators 58, 60 function in the same manner, with the same physical characteristics as the data comparator with the exception of their reference voltage. The high comparator (COMP_H) 58 references the data input signal 54 to a pre-determined high voltage limit (VREF_H). Conversely, the low comparator (COMP_L) 60 references the data input signal 54 to a predetermined low voltage limit (VREF_L).

The output from each comparator feeds into the clock inputs of two separate flip-flop circuits 62a – 62d. Specifically in the embodiment shown, the output of COMP_H 58 feeds into the clock input of first flip-flop 62a and the clock input of the third flip-flop 62c. The output of COMP_H 58 first passes through a delay buffer 68b before being input into the third flip-flop 62c. The output of COMP_L 60 feeds into the clock input of second flip-flop 62b and the clock input of the fourth flip-flop 62d. The output of COMP_L 60 first passes through a delay buffer 68a before being input into the second flip-flop 62b. In

summary, the outputs of COMP_H 58 and COMP_L 60 provide the clock signal for the flip-flops 62a - 62d.

In this embodiment, each flip-flop 62a – 62d has an initial data bit value of "0". This is accomplished by use of a "power on reset" for each flip-flop 62a – 62d which automatically resets the data value to "0" when the circuit 50 is powered up. Upon receipt of a clock signal from COMP_H 58 or COMP_L 60, each flip-flop 62a – 62d will output a "1" to one of the XOR gates 64a, 64b. The output of these gates is then input into the NOR gate 66 and displayed as a flag on the alarm output 70. The value of the flag will then indicate if signal performance is normal or if a noise error has occurred.

As shown in Figure 1A, a normal signal with a digital LOW value will monotonously cross over VREF_L first, then VREF, and finally VREF_H before reaching a digital HIGH value. Conversely, a normal signal with a digital HIGH value with monotonously cross over VREF_H first, then VREF, and finally VREF_L before reaching a digital LOW value. In some embodiments of the present invention, the difference between the high voltage limit and the low voltage limit is 300 mV.

As shown in Figure 2, the circuit 50 may be broken down into two separate sections: a high-to-low section and a low-to-high section. Each section measures one of the transitions of the signal voltage and tests for errors in the transition. The high-to-low section includes the flip-flop 62a, the flip-flop 62b with delay buffer 68a and an XOR gate 64a. This section measures the transition of a signal voltage as it decreases in value through VREF_H, VREF, and VREF_L, respectively. The delay buffer 68a serves to delay the input from CMP_L 60 to

flip-flop 62b in order to prevent an error from too large a transition signal being received.

Conversely, the low-to-high section includes the flip-flop 62c, the flip-flop 62d with delay buffer 68b and an XOR gate 64b. This section measures the transition of a signal voltage as it increases in value through VREF_L, VREF, and VREF_H, respectively. The delay buffer 68b serves to delay the input from CMP_H 58 to flip-flop 62c in order to prevent an error from too large a transition signal being received.

During a signal transition, CMP_H 58 and CMP_L 60 will check the nature of the monotonous signal transition against the pre-set voltage boundaries of VREF_H and VREF_L, respectively. If the transition is normal as shown in Figure 1A, the decision logic of the circuit 50 will drive the value of the flag output to indicate a normal state at the alarm output 70. However, if the transition is in error due to voltage ring back, abnormal voltage levels, etc., the decision logic of the circuit 50 will drive the value of the flag output to indicate an error state at the alarm output 70.

The advantages of the disclosed invention includes the ability of a digital circuit to perform a self-diagnosis of signal noise error without pin-by-pin or other time intensive debugging methods. Another advantage of the disclosed invention includes the ability for the circuit to perform self-diagnosis of signal noise error in the test lab, at production quality control, or during actual usage.

While the invention has been disclosed with reference to specific examples of embodiments, numerous variations and modifications are possible. Therefore, it is intended that the invention not be limited by the description in the specification, but rather the claims that follow.

What is claimed is:

1. An apparatus for detecting a noise error of a signal comprising:

a high comparator that references a high voltage limit with the signal and generates an output;

a low comparator that references a low voltage limit with the signal and generates an output; and

a circuit that processes the high comparator output and the low comparator output, wherein the circuit generates an alarm if a noise error is detected.

2. The apparatus of claim 1, wherein the circuit comprises:

a high-to-low sub-circuit that detects a noise error during a rising signal transition; and

a low-to-high sub-circuit that detects a noise error during a falling signal transition.

3. The apparatus of claim 2, wherein the high-to-low sub-circuit and the low-to-high sub-circuit each comprise:

a plurality of flip-flop circuits;

a delay buffer; and

an XOR logic gate.

4. The apparatus of claim 1, wherein the high comparator and the low comparator each comprise a differential amplifier.

5. The apparatus of claim 1, wherein the high comparator and the low comparator each comprise a sense amplifier.

6. The apparatus of claim 1, wherein the difference between the high voltage limit and the low voltage limit is 300 mV.

7. An apparatus for detecting a noise error of a signal comprising:

a high comparator that references a high voltage limit with the signal and generates an output;

a low comparator that references a low voltage limit with the signal and generates an output, wherein the difference between the high voltage limit and the low voltage limit is 300 mV;

a high-to-low sub-circuit that detects a noise error during a rising signal transition, wherein the high-to-low sub-circuit comprises,

a plurality of flip-flop circuits;

a delay buffer; and

an XOR logic gate;

a low-to-high sub-circuit that detects a noise error during a falling signal transition, wherein the low-to-high sub-circuit comprises,;

a plurality of flip-flop circuits;

a delay buffer; and

an XOR logic gate; and

wherein either sub-circuit generates an alarm if a noise error is detected

8. An apparatus for detecting a noise error of a signal comprising:

means for detecting a high voltage noise error;

means for detecting a low voltage noise error; and

means for activating an alarm signal upon detection of the high voltage or the low voltage noise error.

9. A method for detecting a noise error of a signal comprising:

comparing a high signal voltage with a high voltage limit;

activating an alarm if the high signal voltage is less than the high voltage limit;

comparing a low signal voltage with a low voltage limit; and

activating an alarm if the low signal voltage is greater than the low voltage limit.

10. The method of claim 9, wherein the difference between the high voltage limit and the low voltage limit is 300 mV.

11. The method of claim 9, wherein the low signal voltage is compared with the low voltage limit by a low-to-high sub-circuit that detects the noise error during a falling signal transition, wherein the low-to-high sub-circuit comprises,

a plurality of flip-flop circuits;

a delay buffer; and

an XOR logic gate.

12. The method of claim 9, wherein the high signal voltage is compared with the high voltage limit by a high-to-low sub-circuit that detects the noise error during a falling signal transition, wherein the low-to-high sub-circuit comprises,

a plurality of flip-flop circuits;

a delay buffer; and

an XOR logic gate.

13. A method for detecting a noise error of a signal comprising:

comparing a high signal voltage with a high voltage limit using a high-to-low sub-circuit that detects the noise error during a falling signal transition, wherein the low-to-high sub-circuit comprises,

a plurality of flip-flop circuits,

a delay buffer, and

an XOR logic gate;

activating an alarm if the high signal voltage is less than the high voltage limit;

comparing a low signal voltage with a low voltage limit using a low-to-high sub-circuit that detects the noise error during a falling signal transition, wherein the low-to-high sub-circuit comprises,

a plurality of flip-flop circuits,

a delay buffer, and

an XOR logic gate; and

activating an alarm if the low signal voltage is greater than the low voltage limit.

NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC

ABSTRACT

A noise margin self-diagnostic receiver circuit has been developed. The self-diagnostic circuit includes one comparator for comparing the signal voltage to a high reference voltage, a second comparator for comparing the signal voltage to a low reference voltage, and a logic circuit that activates an alarm if a noise error is detected. The circuit analyzes the data from the comparators and determines if a noise error has occurred.

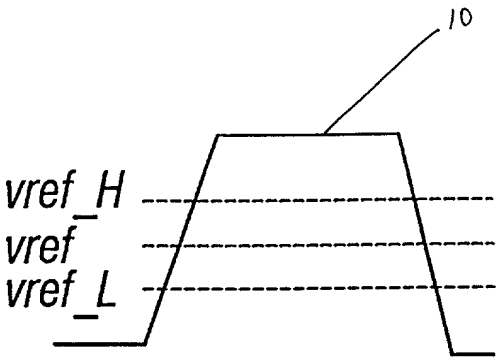

FIG. 1A

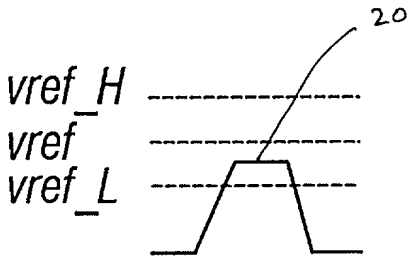

FIG. 1B

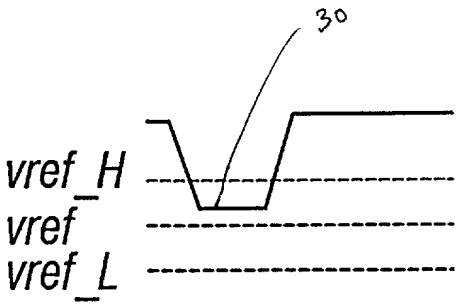

FIG. 1C

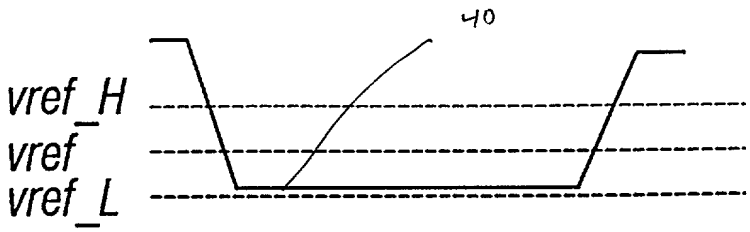

FIG. 1D

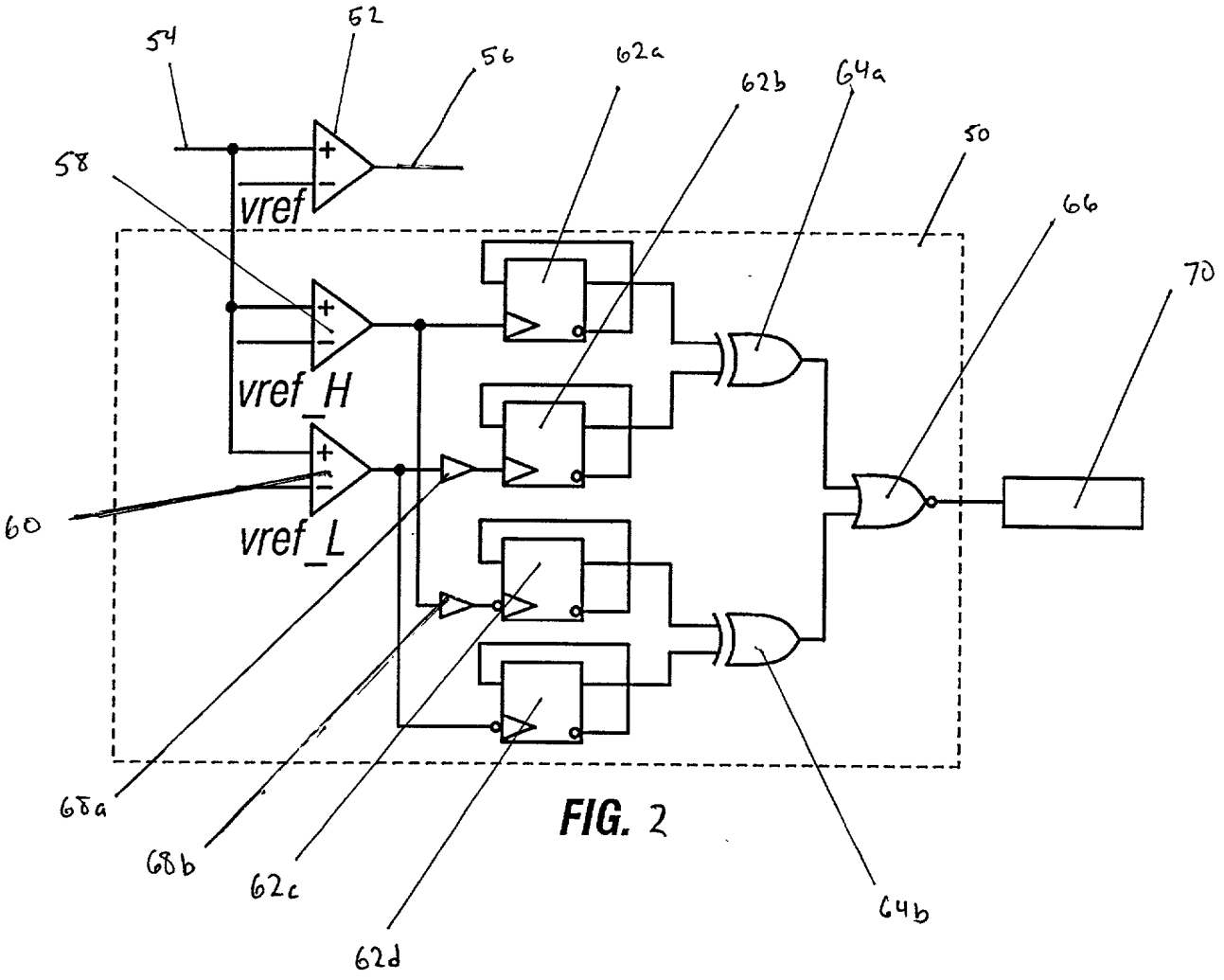
54
52
56
62a
62b
64a
50
58
vref
66
70
vref_H
60
vref_L
68a
68b
62c
62d
64b

FIG. 2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

POWER OF ATTORNEY

Docket No.
P4928/06145.003001

Name of Applicant: **SUN MICROSYSTEMS, INC.**
Address of Applicant: **901 San Antonio Road, MS-PALOI-521**
Palo Alto, California 94303

Title: **NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC**

Serial No., if Any:

Filed:

TO THE ASSISTANT COMMISSIONER FOR PATENTS

The Assistant Commissioner for Patents
Washington, D.C. 20231

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I hereby appoint:

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Kenneth Olsen , Reg. No. 26,493; Timothy J. Crean, Reg. No. 37,116; Robert S. Hauser, Reg. No. 37,847; Joseph T. FitzGerald, Reg. No. 33,881; Alexander E. Silverman, Reg. No. 37,940; Christine S. Lam, Reg. No. 37,489; Anirma Rakshpal Gupta, Reg. No. 38,275; Sean P. Lewis, Reg. No. 42,798; Michael J. Schallop, Reg. No. 44,319; Bernice B. Chen, Reg. No. 42,403; Kenta Suzue, Reg. No. 45,145; Noreen Krall, Reg. No. 39,734; Richard J. Lutton, Jr., Reg. No. 39,756; Monica Lee, Reg. No. 40,696; Marc D. Foodman, Reg. No. 34,110, and Naren Chaganti, Reg. No. 44,602, of SUN MICROSYSTEMS, INC.

as principal attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

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Kenneth Olsen, Reg. No. 26,493
Vice President Intellectual Property
Sun Microsystems, Inc.
901 San Antonio Road, M/S PAL01-521
Palo Alto, Ca 94303

Dated: OCT 18 2000

Docket No.
P4928/06145.003001

Declaration For Patent Application

English Language Declaration

22511
PATENT TRADEMARK OFFICE

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

NOISE MARGIN SELF-DIAGNOSTIC RECEIVER LOGIC

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, CFR Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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